Electronics Status and Issues

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FE Electronics Status and Planning:

- Major discussions for TEMIC and 0.25μ planning to discuss.

Issues related to Services Connections:

- Discussed new concept for opto-link location, PP0, power supply definition, etc.

Power Supplies:

- First results from CAEN prototype, potential second vendor, interest from OSU.

Test Systems for Production:

- Surveyed present status and plans.

Off-Detector Electronics:

- Significant progress towards prototypes, but little involvement from pixel groups.

FE Electronics Planning

Discuss next steps with FE-D2 and TEMIC

- Expected “wafers out” date from TEMIC is Oct. 16 (week 42), one week later than originally foreseen. Still waiting for detailed confirmation.
- Many things to synchronize (testing of all parts, possible irradiations, etc.)

Situation with Honeywell SOI

- New cost information received, indicating cost increase of factor roughly 2.5, making this process un-affordable for ATLAS pixels.

Combination of yield and technology problems with DMILL and cost increases from Honeywell makes it imperative to begin working in 0.25μ technologies:

- There was a 3-day FE workshop in LBL Sept 20-22, where a first discussion of the goals, tasks, and schedules took place.
- There was a more comprehensive workshop at CERN last week (Sept. 27).
- Conclusion was to proceed rapidly with conversions of pixel designs.
- This development is very late, and pushes our schedules to their limits for 2004 delivery of detector to ATLAS.
- We will need to carefully monitor priority/resources for 0.25μ and TEMIC work.

FE-D2 and TEMIC Planning

Two runs in progress with TEMIC:

- Standard 8-wafer engineering run with FE-D2 devices (FE-D2S and FE-D2D, MCC-D2, VDC-P2, DORIC-P2, plus miscellaneous test chips and test structures).
- Experimental 22-wafer run with same reticle, but with corners for three critical variations agreed to by LETI and TEMIC, with the hope of determining the source of the technology problems which caused extremely low yields on FE-D1 chips.
- Wafers to be divided into two identical groups, shipped directly to Bonn and LBL for testing. LBL plans to rapidly test FE chips on one wafer, have it diced, and distribute parts (package 10-25 MCC-D2, distribute bare die for PM-bars, Analog Test Chips, VDC-P2, DORIC-P2, etc.) to design groups for very quick evaluation.

Critical to evaluate this run rapidly:

- For FE chips, goal is first evaluation for Dec pixel week, to decide how to proceed with TEMIC, and how to divide resources between TEMIC and 0.25µ work.
- For MCC-D2, need to understand whether TEMIC is a real vendor, and if not, begin rapid conversion to 0.25µ.
- For VDC/DORIC, indications are that TEMIC could be a vendor, but need to make sure that DORIC works well.

Evaluation steps for FE-D2 Run

FE-D2 evaluation:

- First, study results at wafer probe level in Bonn and LBL. Understand differences between behavior and yield for FE-D2D and FE-D2S.
- If either version of the FE-D2 looks like it operates reasonably well, send wafers for bump-bonding, and also prepare test boards for PS irradiation.
- As soon as “experimental” wafers are available, carry out yield and test measurements for them, and look for “smoking guns” pointing to origin of low FE-D1 yield. Possibly buy some wafers from experimental run for bumping, etc.

MCC-D2 evaluation:

- Genova will already be irradiating MCC-D0 in PS beam in Oct, using newly designed test system for this purpose.
- Will prepare packaged MCC-D2 for Genova as rapidly as possible. Genova will study yield and performance, and decide whether to irradiate in PS this year.

DORIC-P2/VDC-P2 evaluation:

- Dice parts as rapidly as possible and send to Siegen/OSU/Wuppertal for evaluation.
- If they work well, try to irradiate in PS as well ? Lower priority than above...

Test Chips:

- Previous results with Analog Test chips indicated failure after moderate doses, inconsistent with results from single transistors in PM bars. These need to be repeated if possible with the new test chips.
- Previous results with PM bars showed large shifts, but no fundamental problems. These irradiations were performed un-biassed. It would be useful, but not essential, to irradiate more bars with “worst-case” bias (NMOS turned on, PMOS turned off).

Comments:

- Given the very late delivery of the wafers from TEMIC (and they are not delivered yet !), it is extremely difficult to test and prepare parts for testing in the PS run.
- The PS run continues to Nov 13, but we would need to have any new assemblies by approximately Nov 1 in order to be able to expose them to significant doses (one week required to expose device to full pixel fluence). Also, there are presently only 8 slots available in the cold box and so competition for space may be fierce.
- We will do our best to get this ready, but a large coordinated effort from many people will be needed !
- In addition, we are preparing setup to do irradiations at LBL in Dec or later. However, only one board at a time (55 MeV), so not “production” like PS.

Proceeding towards 0.25μ versions of Pixel Chips

Background:

- We now have at most one vendor for our rad-hard designs in pixels.
- We have found that our designs must be more aggressive to fit within the restrictions imposed by DMILL (dynamic logic, little SEU tolerance, operation over very large parameter variations, very large die size, etc.). This requires extra engineering and testing, and there is extra risk.
- This makes it imperative to develop 0.25μ versions of our pixel chips (FE, MCC, VDC, DORIC), or we risk having nothing with which to construct ATLAS.

Topics and Goals for LBL FE-I Workshop:

- Discuss special concerns for using 0.25μ processes - remaining risks ?
- Discuss current FE-H and FE-D designs, and evaluate block by block what changes are necessary or desirable. First agreements on who will do what.
- Discuss technology issues (TSMC vs IBM rules, metal layers, linear caps, etc.)
- Discuss design methods (top-down design, synthesis, CAD tools) and upgrades to design kit (back-annotated Verilog, SEU-tolerant cells, substrate contacts, etc.)
- Do we prototype in TSMC/IBM MPW first or go directly to engineering run ?
- Everyone agreed to proceed as rapidly as possible...

Overview of Issues for FE-I Development

Access to submissions:

- IBM MPW organized by CERN as 3-metal submissions with “fixed” dates. First one relevant for us is tentatively end of Feb. 2001. Turnaround is 10-13 weeks.
- TSMC MPW organized through MOSIS in US. Relevant dates for us are Jan 2 2001, and Feb 26 2001. Turnaround is 8-10 weeks, and cost for 25 small die is \$1550/mm^2, or about 15-20K\$ for Analog Test Chip (about 2x4mm).
- IBM engineering run, nominally 2-6 wafers, but 12 can be possible depending on foundry. Cost for 6 wafer run is approximately 140K\$. Scheduled when we want, and turnaround time is 10-13 weeks. Penalty of 30K\$ if total CERN engineering runs exceed 4 per year. Next step is production run, minimum of 48 wafers and 20 week turn-around.
- Propose to reserve slot in 2Q01 for 6-wafer engineering run in 5-6 metals, in order to make our intentions known to CERN, and begin preparing PO, etc.

Goals of FE-I submission:

- Necessity of extensive testbeam and irradiation tests implies creating chip on the fastest possible schedule. H8 schedule in 2001 extends through the end of October with 2 weeks of 25ns running. An engineering run by June 1 2001 is the latest date to provide wafers and assemblies for these critical evaluation periods.

- Critical path for electronics is to build modules for assembly into “fixed” portions of system, where a “first production wafers” date of about July 1 2002 is vital.
- These are very aggressive schedules...
- A “conservative” design (equivalent to FE-H) is the best match to these goals, and using 50μ x 400μ pixels and 32 EOC buffers is adequate. To maximize chip lifetime and reliability, propose to use 2.0V supplies for VDD and VDDA. Will start from FE-H pinout, and possibly update for power supply connections.

Major Issues for FE-I Conversion:

- Basic idea is to develop conservative chip, like FE-H, based on 400μ pixel, about 32 EOC buffers, and overall with the same basic design.
- Need significant changes in present front-end design for feedback and threshold control, which rely on small W/L NMOS devices which cannot be built in 0.25μ with annular layouts.
- Have significant concerns about SEU tolerance of designs. Several solutions are available (error correcting registers, more robust state machine designs, etc.)
- For digital readout, propose to move towards a fully static readout design, to minimize impact of SEU and leakage.
- Also a new idea to include digital timewalk correction in CEU based on TOT values. This could give us more flexibility in achieving timewalk specs, which have proved marginal and difficult to improve in our present complete chips.

Proposal for Who does What for FE-I

Bonn (Peter, Giacomo, Ivan):

- Responsibility to update cell layout for library to include TSMC compatibility, separate substrate connection, additional pixel-specific cells.
- Conversion of analog blocks from FE-D, including DACs, chopper, and threshold control. Design of Hamming-code correcting registers.
- Responsibility to integrate and submit Analog Test Chip like that included in FE-D submissions. This would be a MPW run with TSMC, targeted for Jan 02, 2001.

CPPM (Laurent, Isabelle, Moshine):

- Responsibility to develop and lay out new analog front end design. Will be on a fast track for TSMC submission, and is presently the critical path.
- Responsibility for design of biassing and threshold control, current reference, analog buffer, and LVDS I/O (if we choose to update the existing standard cells).

LBL (Emanuele, Roberto, Gerrit, Kevin):

- Overall responsibility for design environment and common TSMC/IBM rules.
- Responsibility for updated column pair readout (pixel hit logic, pixel memories, CEU, and sense amps) plus pixel control block, updated EOC buffer design, and integration into complete column pair.

- Responsibility for all digital logic at bottom of chip, which will be almost entirely synthesized and mainly placed and routed with automatic tools.
- Responsibility for overall integration of all blocks into final submission to IBM.

Next Steps for FE-I:

- Believe that critical path will be creation of new front-end design. We have discussed at length how to accelerate this process, but it is difficult.
- Will begin weekly/bi-weekly phone meeting with Bonn/CPPM/LBL to try to work as efficiently as possible.

Inclusion of new members in design team:

- Propose that best role for NIKHEF student is to take over delay cricuit first prototyped by P. Fischer for MCC-D2, and convert and possibly improve it.
- Logical role for Milano (M. Citterio) given experience as analog designer is in front-end, and we will work to include him in design team in analog areas. This will be very challenging...

Conclusions on 0.25μ Work:

- Agreement to proceed on FE-I as rapidly as possible.
- Major issue is how best to create new front-end design. Can either proceed via rapid MPW prototype, followed by engineering run (early delivery of design, but with measurements before full run) or via careful, well-simulated design with no prototype measurements. This requires further study.
- Constraints placed by need to fully characterize and qualify a new design with a new vendor during 2001 suggest an engineering run is required by Jun 1 2001.
- Discussed conversion issues for MCC-D2. Since the design is driven by high-level (Verilog) description, with limited use of full-custom blocks, conversion should be relatively easy. Given needs for continued evaluation of MCC-D0 and MCC-D2 on rapid schedule, would expect to begin real work on this in Jan 2001, with goal of submitting a complete prototype when FE-I is ready.
- Discussed conversion issues for VDC and DORIC. Present groups are eager to begin investigating conversion, and would expect to produce new designs either for an MPW run in early 2001, or for the FE-I engineering run.
- There is potentially a large conflict between resources needed for the work above, and resources needed to develop pre-production quality DMILL versions of the chips in the FE-D2 run. We will re-discuss all of these issues in Dec pixel week, based on first results from characterizing chips from FE-D2 run.

Issues Related to Services Connections

- Significant progress in recent design and prototype efforts in Bonn and LBL.
- These raise many new issues, which were discussed during opto-meeting and module meeting last week.

Some issues:

- Disk services clearly prefer an opto-link design in which the links are pushed out of the pigtail region to what is called PP0. This has many implications.
- One implication is that it is most natural to implement an opto-link at the sector or half-stave level. This means a 7-wide optolink, with a new opto-package and modified opto-electronics. This may be the only way to meet our extreme space constraints as well. This also suggests a significant reduction in the connections from the power supplies to the opto-link. The present VVDC, VPIN, VISET (and also Reset for other reasons) could exist at the opto-package level (factor 6-7 reduction in lines for these services), but this would clearly imply a reduced redundancy in the opto-links.
- A second implication is that if we wish to implement this scheme also in the barrel region, the pigtails are much longer, and we would now be transmitting the critical fast signals (XCK, DCI, DTO) as LVDS signals over up to 1 meter cables, with potentially major system noise and integration implications. Note this could allow moving the links to larger R, reducing total dose and SEU effects significantly.

- Finally, SEU measurements of links at B-layer fluences show a higher than expected BER. The original spec was 10^{-11}. This was degraded to 10^{-9} after initial radiation studies. It now appears to be 10^{-8}. We believe the more robust protocols implemented in the FE-D2 can cope with this error rate for the DCI. Further study is needed of the implications of this high SEU rate for the XCK regenerated by the DORIC, and whether it meets the requirements of the MCC and FE chips.

Comments:

- In the module meeting, strong support was given to prototyping these new solutions. This means specifying and developing a new 7-wide opto-link (first discussions with the Taiwan group indicate their willingness to work with us on this). It also means incorporating the reduced power supply connections into the evolving PP0 prototyping program, to investigate grounding and redundancy issues. At some point, it would lead to revised specifications for the power supplies and for the power cables.
- It is critical to try to assess whether this scheme can also work in the barrel. This requires prototyping the long pigtails required, examining signal quality and noise issues with great care. It also means attempting to build a realistic mock-up of the noise environment which would be created by these pigtails (large number of pigtail bundles operated close to 1-2 modules in a realistic grounding environment ?)

Power Supplies

CAEN Update:

- Delivery of the first CAEN prototype module happened in Sept.
- Module has been briefly tested, and appears to meet nominal specifications. First attempts to operate a pixel module with it showed serious noise problems, but many subtle issues involved, and additional work is required to understand.

New Vendor: DPS in Meyrin.

- After discussions with Susanne, a detailed proposal has been submitted for fabricating prototype crate, controller, and pixel-specific module for 30 KCHF.
- After discussions in the electronics meeting, we agreed that this proposal should be pursued. The vendor seems knowledgable and competent (albeit small).

Interest from OSU group in developing system:

- OSU has developed power supply systems used in AMY and CLEO, and in particular for the newly installed CLEO silicon vertex detector.
- They have received our specs, and will study them in more detail. Propose that they return in Dec and make a detailed presentation to electronics meeting. Must have schedule of prototype system for evaluation in 6-9 month timescale.

No major issues for 0.25μ chips if current budgets are kept.

Test Systems for Production

- Surveyed status of test systems for electronics components (but 0.25μ, with operation at 1.5-2.0V, still needs further consideration in some designs):

FE Chips and Modules:

- Major upgrade of PLL system under way at LBL. Behind initial schedule, but now approaching completion. Addresses all production needs for chips and modules.

MCC and Flex Testing:

- Present MCC test system build by Genova will address Flex testing needs, and most MCC characterization and debugging needs.
- Production plan involves use of IMS IC Tester at CERN. First experience will be gained with using this machine to test MCC-D2. If it is not adequate, other possibilities would include looking for a commercial vendor to test the chips.

DORIC, VDC, and opto-link and opto-harness testing:

- Major ingredients for this are BER testers. Some prototypes exist, but thinking about production issues is just beginning.

Overall:

- Many uncertainties exist about production reliability requirements, in particular developing/qualifying the KGD and burn-in protocols to be used for components.

Off-detector Electronics

Significant progress towards first prototypes:

- Complete ROD Crate must include: Backplane, TIM, ROD, BOC, plus RCC.
- First prototypes for all of these components are now in fabrication, and should be complete and undergoing system integration by the end of this year.
- The nominal schedule involves a user evaluation period, lasting into the middle of 2001 to test these modules in the SCT and Pixel communities, and provide feedback to designers for pre-production version.

Present Pixel Evaluation plans involve:

- Extensions of PixelDAQ to test these modules in the lab with real pixel modules (presumably interfaced through copper not glass).
- These modules should be evaluated in a test beam environment next year.
- Believe that more significant involvement of groups outside LBL is needed to evaluate these modules, and become generally knowledgable about ROD.
- A related issue is the DAQ software development required to implement DAQ-1 in the H8 testbeam, and in ATLAS. Presently, only UIowa is working in this area, and additional manpower will certainly be needed in the future.
- Would like to see other groups make commitments in near future !